Thermal Analysis of Integration of DC/DC & DC/AC Inverter Stages

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Abstract: The temperature distribution and flow field velocity is shown from the current heat sink design. A 3D model is built and we reveal the relationship of the maximum cooling temperature of chip with the design geometry of heat sink such as substrate thickness, fin height and fin thickness by passive natural convection and radiation cooling. A small scale experiment, where a 10mm × 10mm× 2mm thick small heater is attached to the bottom of a 50mm×50mm×20mm high aluminum heat sink, proves the accuracy of our calculation. Our analysis shows that the current design can be improved in respect of reduction of weight.

I. Current and Old Design Comparison

1. The Inverter Stages

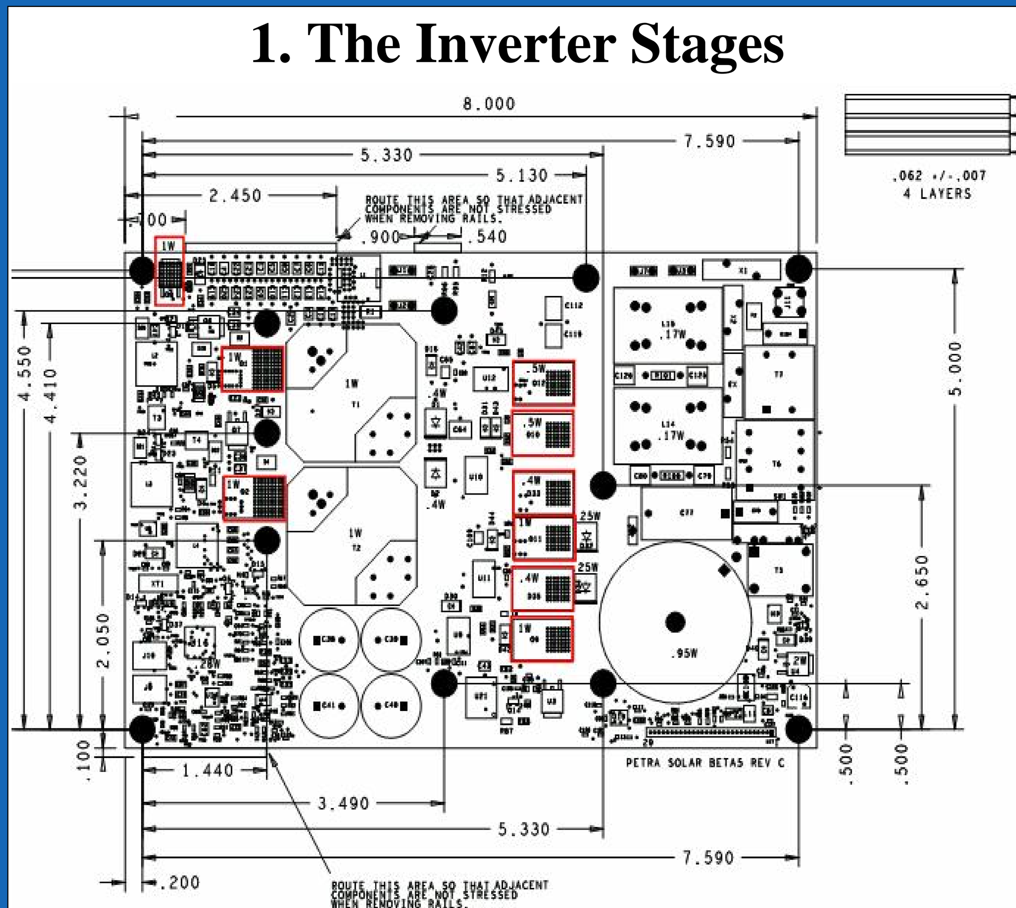


FIG. 1a. Illustration drawing of the system.

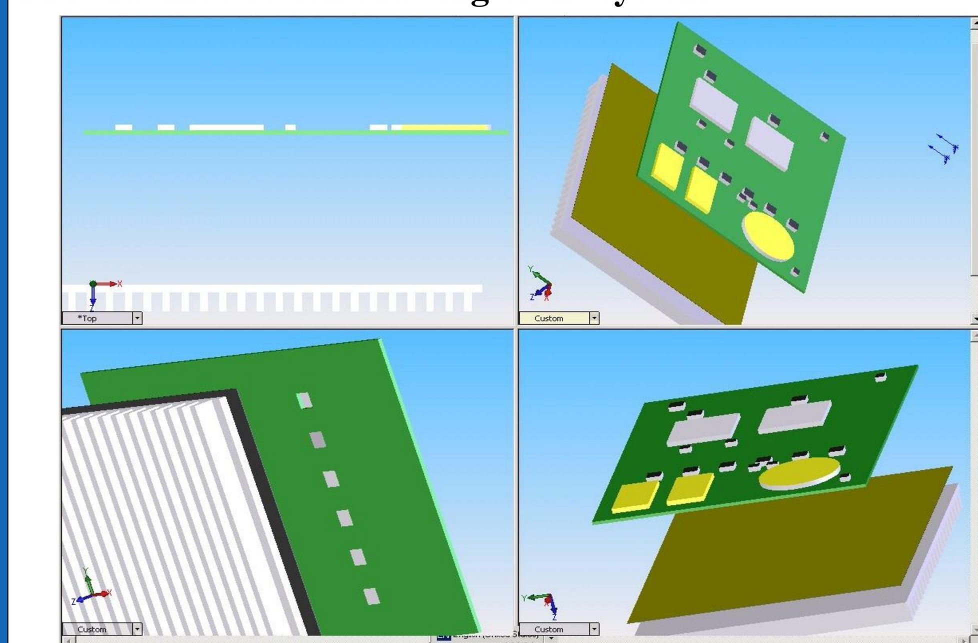
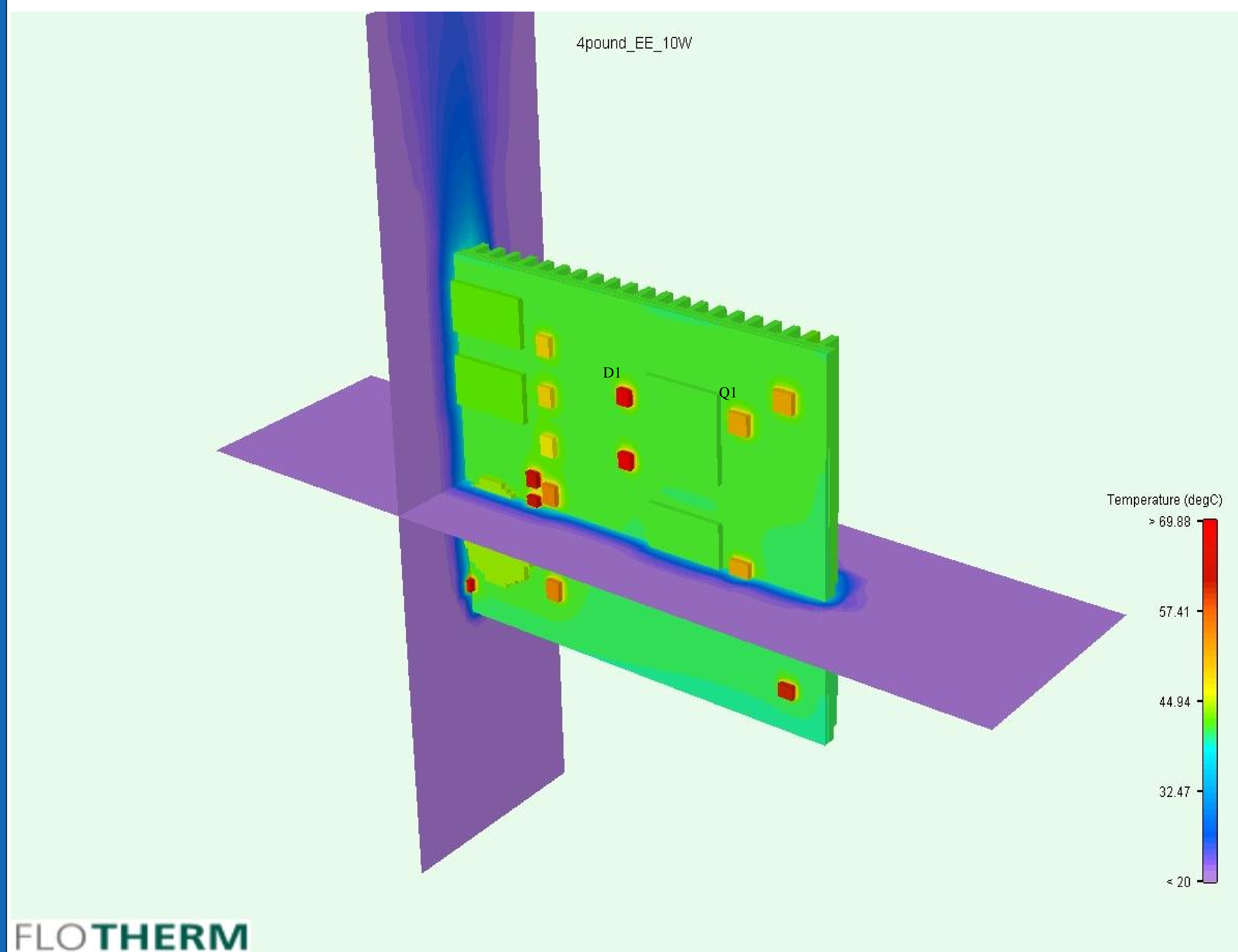


FIG. 1b. the PCB assembly.

REF DES	PACKAGE	POWER	THERMAL VIAS
Q 1	D2PAK	1 W	Y
Q 2	D2PAK	1 W	Y
T 1	RM14 CORE	1 W	N
T 2	RM14 CORE	1 W	N
Q 9	D2PAK	1 W	Y
Q 11	D2PAK	1 W	Y
Q 10	D2PAK	.5 W	Y
Q 12	D2PAK	.5 W	Y
D 2	SMC	.4 W	N
D 1	SMC	.4 W	N
U 4	DPAK	.25 W	N
D 34	SMC	.25 W	N
D 32	SMC	.25 W	N
D 35	D2PAK	.4 W	Y
D 33	D2PAK	.4 W	Y
L 9	42/29 POT CORE	.95 W	N
L 14	EV28 CORE	.165 W	N
L 15	EV28 CORE	.165 W	N
U 16	44 TQFP	.28 W	N
Q 8	DPAK	2 W	Y

FIG. 1c. Power consumption of chip on the board

2. The maximum cooling temperature of chip



The old aluminum heat sink is simulated (200mm×150mm×3mm).

A 0.3-mm thick High thermal conductivity Thermal Interface Insulation Pad (HTIP) is used to provide electrical isolation. (Thermal conductivity k=1.2W/m.K).

Each of the 22 fins has dimensions of 150mm×3.5mm×10mm. The distance between fins is 8.5mm (center to center).

High power MOSFET (Q1 etc), producing 1 W of heat, is simulated as a small chip with dimensions of 8mm×6mm×3mm with thermal vias. Similarly, each DIODE (D1 etc), producing 0.4W of heat, is simulated as a small chip but without vias. In an ambient environment of 20°C with heat dissipation by passive free convection and radiation, the maximum temperature occurs at the DIODE but not at the MOSFET because it is helped by thermal vias (it is thermally connected to the aluminum heat sink).

The figure above shows a typical result obtained with FLOTHERM. We optimized our design to reduce the weight of heat sink by its Command Center™.

3. Temperature comparison

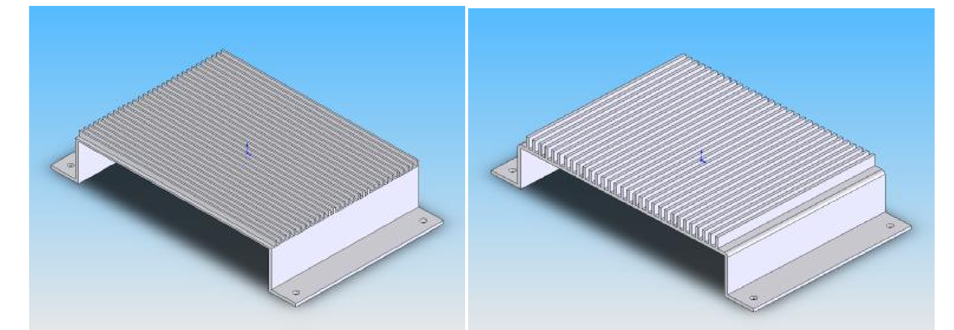


FIG. 2a Current design (left) and old design (Right) which is 220g and 560g respectively.

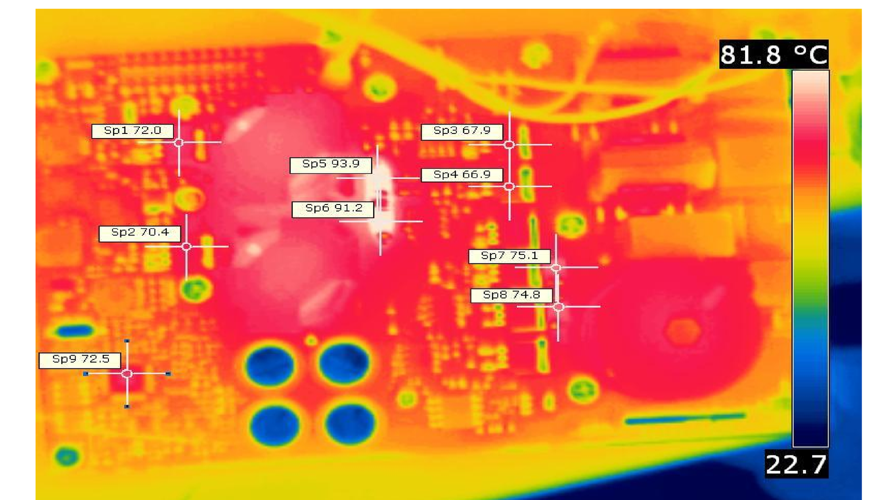


FIG. 2b IR Temperature of current design.

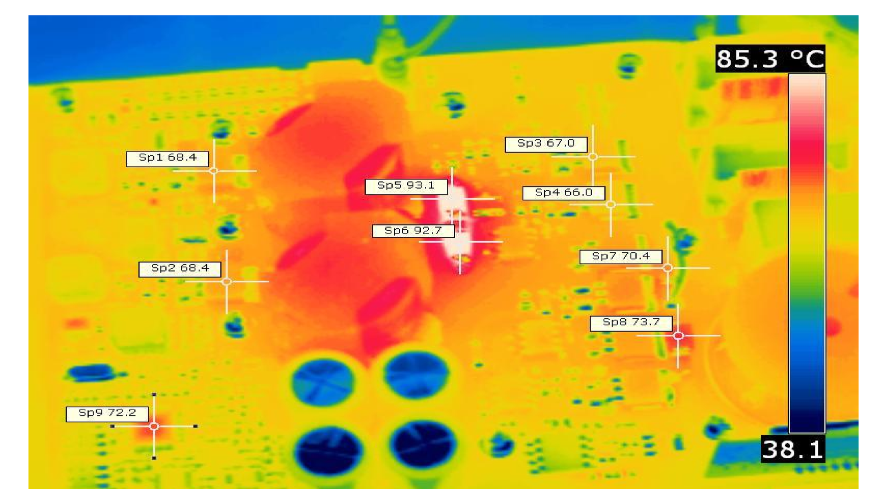


FIG. 2c IR Temperature of old design.

In short, the new and old heat sink designs are compared. The new heat sink design combines the features of heat transfer optimization along with structure strengthening which is about 5 times stronger than the previous design with less weight.

II. Analysis of a Small Scale Experiment

1. The experiment setup

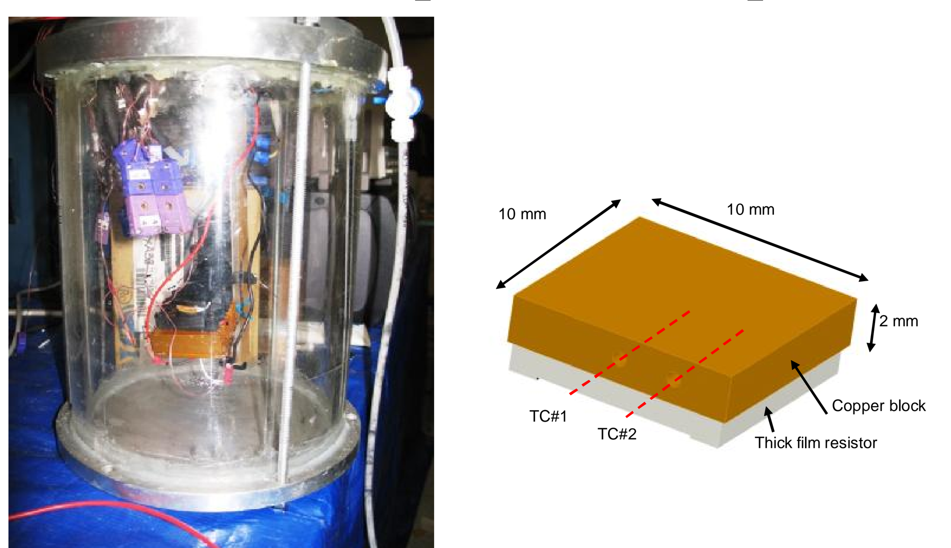


FIG. 3a. The setup overview (Al heat sink, chamber, heater, thermocouples).

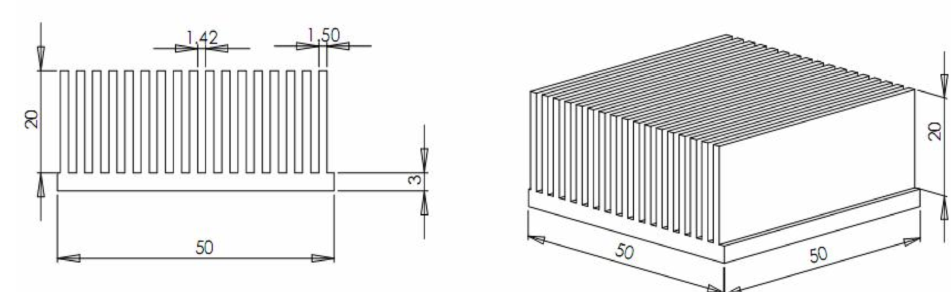


FIG. 3b. Experimental heat sink size.

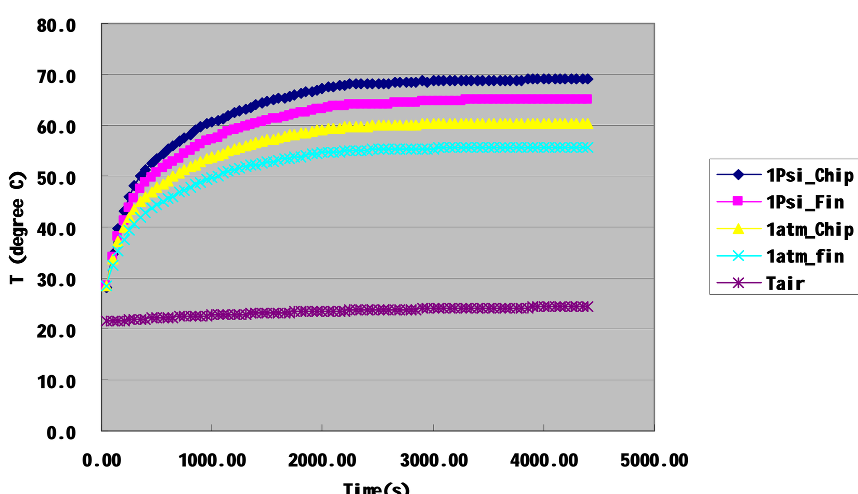
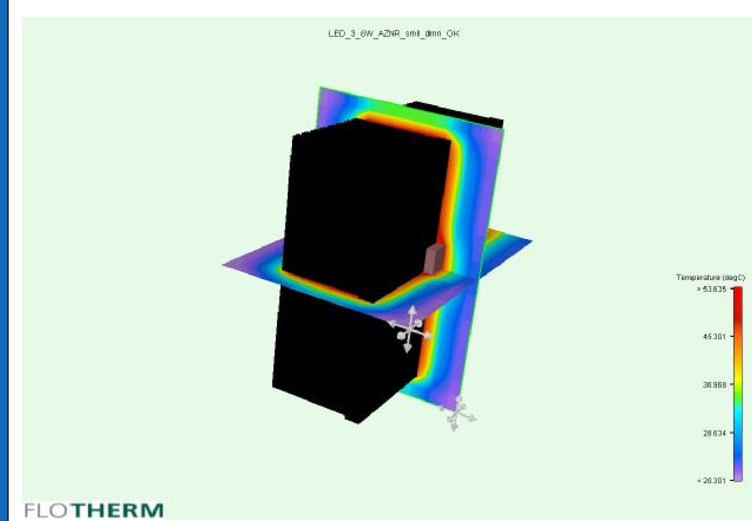


FIG. 3c. It took 4500 second to reach the steady state. This is a typical heating curve.

2. Comparison of experiment and FLOTHERM result

The FLOTHERM results were validated experimentally with the chips simulated by thick film resistors. Figure 3 shows an acrylic chamber which was used to produce a suitable ambient temperature for the heat sink.



Note: In the left figure, the heat sink is in black because it is supposed to use anodized aluminum instead of shiny aluminum. The anodized surface radiation can help to reduce the temperature from 79.4°C to 53.8°C.

Pressure	P(W)	T_{cntr}(°C)	T_{Ambnt}(°C)	DT_chip(°C)	Flotherm(°C)	Flotherm_DT(°C)	Error(%)
1atm	3.6	53.8	23.0	30.8	52.8	32.8	6.10
1atm	7.2	79.7	27.7	52.0	73.2	53.2	2.26
1psi	3.6	63.6	24.0	39.6	62.1	42.1	5.94
1psi	7.2	100.3	28.3	72.0	93.3	73.3	1.77

FIG. 4 The highest chip temperature is 53.8 °C. The base bottom surface area is 25 cm². And the extended fin surface area is approximately up to 250 cm². The ambient temperature is 20°C, and we note that radiation plays an important role in the heat transfer. The fin temperature is almost in uniform.

FIG. 5 The results for the other simulation cases are compared with experimental results in the above figure too. Here, T_{cntr} is the experimental chip center's temperature. T_{ambnt} is the measured ambient temperature. The average error for the FLOTHERM simulation is 4%.

FLOTHERM predicts well with a 3.6W chip heat dissipation with the ambient air at 1 atm and 20°C, the maximum chip temperature is 53.8°C. Considering the complexity of the problem (with heat conduction, buoyancy induced convection and radiation), the agreement is quite satisfactory. We have done additional simulations by assuming the ambient temperature at 1atm to be 79°C. Also, we also performed the case at a pressure of 1 psi. We can change the substrate thickness only to see the effect of substrate thickness. Similarly, we get the temperature increase vs. the vias thermal conductivity. They behaved like an exponential decay, therefore, too thick substrate is not needed.

3. Future work

We note that it is 156°C if we shrink the chip size to be 3×3×0.5 mm. The temperature increase can be explained by the "size effect"---that for the same power consumption, the smaller chip we choose the higher temperature of the chip will be.

Therefore, we need to enhance the heat dissipation from a MOSFET chip through thermal vias. The future investigation will focus on estimating an equivalent thermal resistance between the case of the MOSFET and the heat sink under an optimal thermal via configuration.

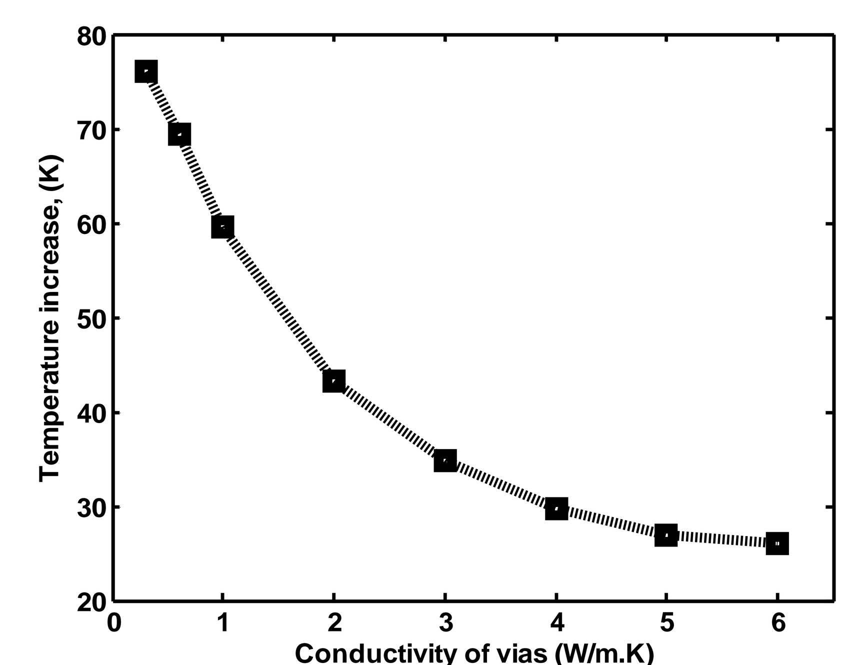


FIG. 6 The maximum temperature increase vs. equivalent conductivity of thermal vias.

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