Materials Science in Semiconductor Processing 12 (2009) 151–155

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Stability of Cu/Ir/Si trilayer structure to moderate annealing

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ARTICLE INFO

Available online 17 October 2009

Keywords:
Iridium
Diffusion barrier
Cu-interconnects

ABSTRACT

The properties and behavior of trilayer structures consisting of ultrathin iridium thin films sandwiched between Cu and Si have been examined. Iridium thin films (5 nm thick) were deposited on Si substrates using magnetron sputtering, followed by in situ deposition of Cu. The film stacks were examined both as-deposited and after annealing in vacuum over a temperature range of 300–600 °C for 1 h. X-ray diffraction indicates that there is no copper silicide formation upon annealing up to 400 °C. Cross-section HRTEM and EDS line-scans on the sample annealed at 400 °C show the out-diffusion of iridium and the onset of copper diffusion across the interface. The results indicate that iridium is moderately effective as a copper diffusion barrier so long as the processing temperatures remain relatively low.

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1. Introduction

Diffusion barriers and buffer layers play a pivotal role in many technologies [1–16]. In electronics, one of the most important issues involves the compatibility of metals used for providing contacts and device interconnects. The ever-increasing suite of active materials together with increased demands on circuit performance creates a significant need to understand the limitations of specific metal interface systems in terms of the materials and processing conditions. As an example, the continuous reduction in Si device feature size will soon out-strip the utility of metallization schemes that employ a tantalum/tantalum nitride (Ta/TaN) diffusion barrier with a Cu seed layer on top for copper metallization. The development of new barrier material structures will be needed as the device dimensions continue to scale down [17–21]. In addition, the conventional Cu electroplating approach for Cu-interconnects requires a Cu seed layer due to the poor nucleation of electrodeposited Cu on Ta [22]. The decreasing feature sizes and increasing high aspect ratios are creating new difficulties in achieving the required uniformity of the Cu seed. As such, the direct copper electroplating on the diffusion barrier without the use of a seed layer has become increasingly attractive. Noble metals, including Ru, Pd, Pt, Rh, Ir, Ag, and Os, have been suggested as replacement materials for the barrier [23], and direct copper electroplating with excellent conformity has been successfully demonstrated for Ru [24], Os [25], and Ir [26]. However, each has its limitations. Recent studies on Ru/Si thin films suggest that Ru itself is not a good barrier against copper diffusion [27–29]. Arunagiri et al. [29] reported that a 5 nm Ru thin film is effective as a copper diffusion barrier only for temperatures up to 300 °C. When one extends the discussion to metallization challenges in even more complex material systems, the need to consider the behavior of specific metal/metal or metal/non-metal interfaces becomes even more apparent.

As one of the platinum group metals, iridium is potentially useful in metallization for a number of electronic applications. It has a high melting point of 2446 °C and low resistivity of 4.71 μΩ cm. Iridium has an

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doi:10.1016/j.mssp.2009.09.008

attractive property of forming a metal oxide (IrO_2) when oxidized. For the metallization of functional oxides, this property is particularly advantageous. As such, understanding the interfacial stability limitations is important. Previous efforts have included the use of Ir as a single component metal, as a single component barrier, and as a barrier in conjunction with other materials. For $Cu–SiO_2$-based electrochemical metallization of memory cells, Ir has been employed as an electrode material [30]. Iridium has been examined as a barrier material for the integration of ferroelectric $Pb(Zr,Ti)O_3$ films on silicon [31]. Iridium has been used in the formation of stacked $SrBi_2Ta_2O_9$ ferroelectric capacitors [32]. Iridium has also been examined as an oxygen barrier for the growth of epitaxial superconducting oxides on metals [33]. Iridium is relatively stable when in contact with Cu with no intermediate compound formation and negligible solubility at high temperatures as shown in the Cu–Ir binary phase diagram [34]. Although these physical properties suggest that iridium could provide utility in metallization for various semiconductors, few investigations have been reported on the properties of iridium as a barrier against copper diffusion. In this paper, the properties and stability of Cu/Ir/Si trilayers is examined.

2. Experimental description

Iridium thin films were deposited on Si(1 0 0) wafers by magnetron sputtering at room temperature. Film thickness was 5 nm. Prior to deposition, the substrate was etched in 7:1 buffered oxide etch to remove the native oxide, followed by a deionized water rinse. The base pressure of the chamber was of the order of 5×10^{-7} Torr and the working pressure was kept at 5 mTorr throughout the deposition. The DC sputtering power for the 3 in Ir target was 100 W. Under such conditions, the measured deposition rate was 0.95 Å/s. During the deposition process, the substrates were rotated at 20 rpm to ensure film uniformity.

A 200-nm-thick Cu layer was deposited on top of the iridium barrier in situ at room temperature without breaking the vacuum. The forward sputtering power for Cu deposition was 200 W. The chamber pressure was kept at 5 mTorr Ar throughout the process. The stability of the structure was examined by annealing in vacuum (10^{-5} Torr) over a temperature range of 300–600 °C for 1 h. The film crystallinity and intermetallic phase formation were determined using a Philips APD 3720 X-ray diffractometer (XRD). The interfacial stability of the film stack and copper depth profile were examined using a JEOL 2010F high-resolution transmission microscope (HRTEM) along with a JEOL Superprobe 733 energy-dispersive spectrometer (EDS). For the characterization of electrical properties, a four-point probe was used to measure the sheet resistance of the film stacks.

3. Results and discussion

Fig. 1 shows the X-ray diffraction patterns for the Cu/Ir(5 nm)/Si structures both as-deposited and annealed

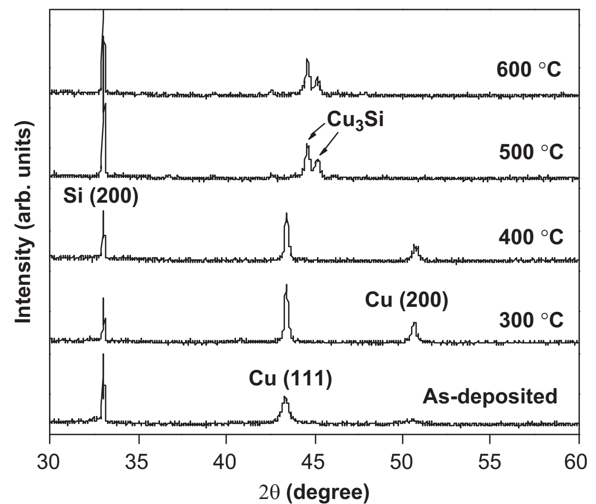

Fig. 1. X-ray diffraction patterns of as-deposited and annealed Cu/Ir(5 nm)/Si (0 0 1).

in the temperature range of 300–600 °C for 1 h in vacuum. As evident from Fig. 1, upon annealing at 400 °C, no copper silicide diffraction peaks are present, implying no significant copper diffusion through the iridium barrier. This reveals that the diffusivity of copper in iridium is relatively low at 400 °C. Due to grain growth upon heat treatment, copper film crystallinity improves as evidenced by the narrowing of the Cu (111) and (2 0 0) peaks. Further annealing yields copper diffusion through the barrier and the formation of copper silicide as indicated by the presence of copper silicide diffraction peaks in the 500 °C annealed samples.

Fig. 2 shows the HRTEM images of the Cu/Ir (5 nm)/Si film stacks before and after annealing at 400 °C for 1 h. As shown in the as-deposited sample, the thickness of Ir barrier is approximately 5 nm. Note that a 2 nm amorphous interlayer lies between the Ir and Si. This amorphous layer is iridium silicide formed at room temperature [35,36] by the diffusion of silicon into iridium [37]. High temperature annealing causes iridium to diffuse further into the adjacent silicon and copper layers as evidenced by the expansion of the dark iridium region shown in Fig. 2b. In agreement with the XRD data, no copper silicide formation is seen in the HRTEM image at the interface upon annealing at 400 °C.

The EDS atomic depth profiles of the as-deposited film stack are shown in Fig. 3. As clearly seen in the depth profiles, a narrow and sharp iridium peak lies between copper and silicon. The EDS Cu signal declines sharply at the position of iridium peak, indicating no copper diffusion into silicon at room temperature. However, a noticeable overlap of silicon and iridium signals exists in the profile as a result of the diffusion of silicon into iridium. The formation of iridium silicide occurs at room temperature. For the annealed stack shown in Fig. 4, the iridium signal spreads towards both silicon and copper. High-temperature annealing leads to perturbation of the iridium bonding, which results in

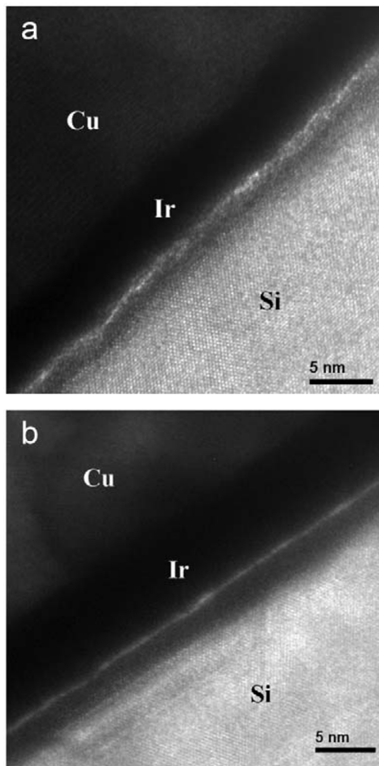

Fig. 2. HRTEM images of Cu/Ir(5 nm)/Si (0 0 1) (a) as-deposited and (b) annealed at 400 °C for 1 h.

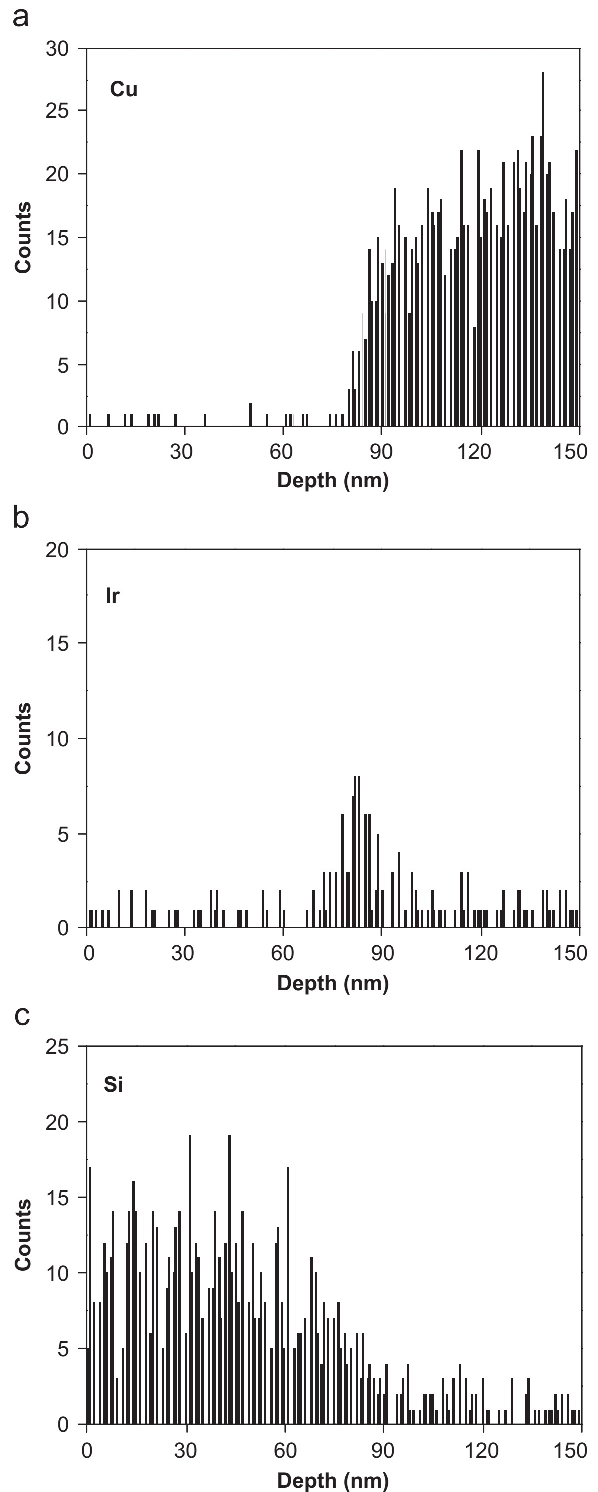

Fig. 3. EDS depth profile of as-deposited Cu/Ir(5 nm)/Si (0 0 1) stack showing the EDS line profile for (a) Cu, (b) Ir, and (c) Si.

the out-diffusion of iridium and further silicidation. In this case, the copper intensity profile declines gradually as the scan moves into the Si substrate and returns to its baseline. The iridium intensity also decreases to its baseline. This result indicates the effectiveness of an ultrathin iridium barrier as a copper diffusion blocking layer on Si for moderate temperature processing.

The sheet resistance of Cu for the barrier stack before and after annealing is shown in Fig. 5. Due to grain growth upon annealing, Cu sheet resistance decreased slightly with increasing temperature until the copper diffusion through the barriers took place. A noticeable increase of Cu sheet resistance occurred at 500 °C as a result of copper diffusion through the barrier and the formation of copper silicide.

4. Conclusion

In summary, the behavior of an ultrathin iridium layer separating Si from Cu was investigated. X-ray diffraction data show that the barrier stack does not fail after annealing at 400 °C for one hour as no copper silicide diffraction peaks are observed. HRTEM images and EDS cross-section line-scans reveal the formation of iridium silicide in the Ir/Si interface at room temperature. The EDS copper depth profile indicates limited blocking of copper diffusion by the iridium barrier upon annealing at 400 °C. Further heating results in iridium out-diffusion and formation of a less-dense iridium barrier, leads to the failure of the barrier at higher annealing temperatures. Overall, the results indicate that 5 nm Ir is an effective barrier against copper

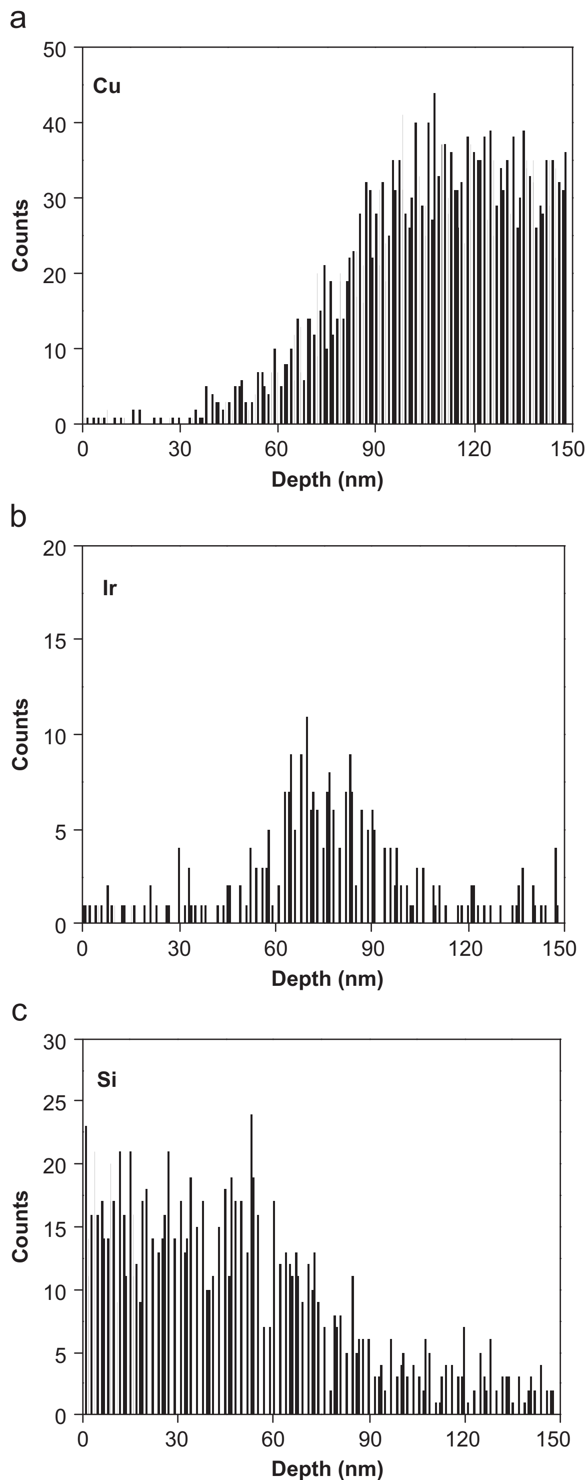

Fig. 4. EDS depth profile of Cu/Ir(5 nm)/Si (0 0 1) stack annealed at 400 °C for 1 h showing the EDS line profile for (a) Cu, (b) Ir, and (c) Si.

diffusion upon annealing at moderate (<400 °C) temperatures. This may prove useful for specific applications in which the thermal processing1 following metallization is consistent with the 400°C limitation.

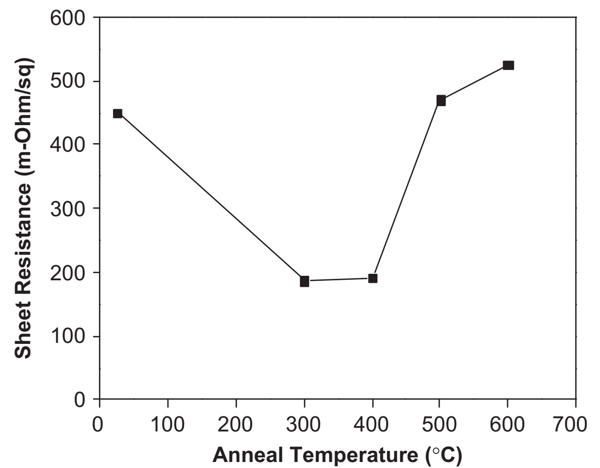

Fig. 5. Sheet resistance of Cu vs. annealing temperature for Cu/Ir(5 nm)/Si.

Acknowledgements

The above work was supported by the National Science Foundation under Grant No. CHE-0304810. The authors would like to acknowledge the Major Analytical Instrument Center, Department of Materials Science and Engineering, University of Florida where the characterizations were carried out. They would also like to thank Ivan Kracachenko and Bill Lewis at the University of Florida Nanofabrication Facility for their assistance with sputtering.

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